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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/639,942	ROBERT H. DENNARD	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13-18* is/are rejected.

7)☒ Claim(s) *12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Lynne A. Gurley

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the application filed on 8/13/03. Currently, claims 1-18 are pending.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4-6 recite the limitation "said bonded structure", in line 1 of each of the claims. There is insufficient antecedent basis for this limitation in the claims. For the purpose of examination on the merits, the Examiner has regarded "said bonded structure" as the "carrier wafer" in claim 1.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3, 5, 13-16, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Neudeck et al. US Patent 5,273,921.

Neudeck discloses the semiconductor method as claimed. See figures 1A-3J, and corresponding text, pertaining to claim 1, where Neudeck teaches a method of fabricating a semiconductor device comprising the steps of: providing a structure comprising a carrier wafer **11**, an oxide layer **12** positioned on the carrier wafer, a polySi back-gate **14** located on the oxide layer, a back-gate dielectric **12** (figure 1B) located on said polySi back-gate and a Si-containing

layer **18** located on said back-gate dielectric; forming a channel region **18** (col. 5, lines 24-27) into a portion of said Si-containing layer; forming a front gate region comprising a front-gate dielectric **19** , front polySi gate **20** and sacrificial spacers **25** (figure 1F) atop said channel region; forming undercutting shallow trench isolation regions **14A, 14B** (figure 1F; see figure 1G for oxide 27 filling regions 14A and 14B) in said structure; removing the sacrificial spacers and forming source/drain extensions **31A, 32A, 31, 32** (figure 1H; 31A and 32A are grown as extensions from channel 18, col. 6, lines 20-31) into the channel region; and forming gate spacers **23** atop the top of the channel region and source/drain regions in said channel region, wherein said polySi back-gate is self-aligned with the front polySi gate and the source-drain extensions (see figure 1H).

Pertaining to claim 3, Neudeck teaches the method, wherein said back-gate dielectric is formed on the Si-containing layer of an initial silicon-on-insulator (SOI) substrate by a thermal growing process or deposition. (col. 1, lines 7-10; col. 5, lines 12-17)

Pertaining to claim 5, Neudeck teaches the method, wherein said Si-containing layer is said bonded structure is thinned by a planarization process. (col. 5, lines 24-28)

Pertaining to claim 13, Neudeck teaches the method, wherein said sacrificial spacers are removed utilizing a chemical etchant. (col. 6, lines 16-18)

Pertaining to claim 14, Neudeck teaches the method, wherein said gate spacers are formed by deposition and etching. (col. 5, lines 46-49)

Pertaining to claim 15, Neudeck teaches the method, wherein said source/drain regions are formed by ion implantation and annealing using the gate spacers as an implanted mask. (col. 25-30)

Pertaining to claim 16, Neudeck teaches the method, further comprising forming raised source/drain regions **31, 32** on said source/drain regions, said raised source/drain regions are formed by deposition of an epi-Si or Si layer and ion implantation and annealing (col. 6, lines 20-40; ***Note***: the annealing step is considered inherent since electrical activation includes a thermal step such as annealing see *Stanley Wolf and Richard N. Tauber Vol. I, Silicon Processing for The VLSI ERA*, pages 303-308, under *Electrical Activation and Implantation Damage Annealing*).

Pertaining to claim 18, Neudeck teaches the method, further comprising forming an insulating layer having conductively filled contact holes atop the structure. (figure 3J and col. 8, lines 22-24)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Neudeck et al. US Patent 5,273,921 in view of Komatsu US Patent 6,342,717, in further view of *Stanley Wolf and Richard N. Tauber Vol. I, Silicon Processing for The VLSI ERA*.

Neudeck discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 3, 5, 13-16, and 18, under 35 U.S.C. 102(b).

However, Neudeck fails to show, pertaining to claim 2, wherein the polySi back-gate is formed by implanting dopants into a polySi layer that are formed atop the back-gate dielectric and annealing the implanted dopants.

Komatsu teaches in figures, 1-12, and corresponding text, in a similar semiconductor method including a front and back gate device having a SOI substrate, implanting dopants into the polycrystalline silicon layer. (col. 3, lines 1-5; col.7, lines 25-35)

Wolf Vol. I, teaches that electrical activation includes a thermal step such as annealing see *Stanley Wolf and Richard N. Tauber Vol. I, Silicon Processing for The VLSI ERA*, pages 303-308, under *Electrical Activation and Implantation Damage Annealing*).

It would have been obvious to one of ordinary skill in the art to incorporate the implanting into the polySi-back gate formed atop the back-gate dielectric and forming an annealing step, pertaining to claim 2, in the method of Neudeck, according to both the teachings of Komatsu and Wolf, with the motivation of, forming a gate contact used to control current flow within the transistor device. In addition, the impurity type (N-type or P-type) determines whether the back gate is NMOS or PMOS transistor type. Finally, it is well known in the art, as taught by Wolf, that doped impurities are activated by a thermal annealing process.

Claims 4 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neudeck et al. US Patent 5, 273,921 in view of *Stanley Wolf, Vol. II, Silicon Processing for The VLSI ERA*.

Neudeck discloses the semiconductor method substantially as claimed. See the preceding rejection of claims 1, 3, 5, 13-16, and 18, under 35 U.S.C. 102(b). In addition, pertaining to claim 4, in figures 1F-1H, it appears that the nitride, from the spacer formation, and the oxide

from the thermal oxidation step, remain in the seed hole 17, thus making seed hole 17 appear to function as an isolation region.

However, Neudeck fails to show, pertaining to claims 4 and 17, the method wherein the bonded structure further includes deep trench isolation regions, each deep trench isolation region having an upper surface that is coplanar with an upper surface of the Si-containing layer; and the method further comprising forming silicide regions on the raised source/drain regions.

Wolf teaches in pages 45-47 and 144-146, under conventional silicon processing, that shallow trenches are primarily used for isolating devices of the same conductive type, where conventional trench isolation includes filling a trench with an insulating material such as an oxide. Wolf also teaches, conventional techniques of forming self-aligned silicide contacts.

It would have been obvious to one of ordinary skill in the art to incorporate the claimed method, wherein the bonded structure further includes deep trench isolation regions, each deep trench isolation region having an upper surface that is coplanar with an upper surface of the Si-containing layer and to have further incorporated forming silicide regions on the raised source/drain regions, pertaining claims 4 and 17, in the method of Neudeck, according to the teachings of Wolf, with the motivation that, since, conventional shallow trench isolation includes filling the trench with an insulating material, one of ordinary skill in the art could replace the seed hole, including the nitride and oxide material, with a deeper trench for the purpose of creating an improved, deep trench isolation region increasing the reliability of the devices. In forming the silicide regions, one of ordinary skill in the art would use the silicide, taught by Wolf, with the motivation that, the silicide decreases the resistance of the contact with the source/drain regions within the transistor device.

Claims 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Neudeck et al. US Patent 5,273,921 in view of Komatsu US Patent 6,342,717.

Neudeck discloses the semiconductor method substantially as claimed. See preceding rejection of claims 1, 3, 5, 13-16 and 18, under 35 U.S.C. 102(b). In addition, pertaining to claim 6, Neudeck teaches the method, where the bonded structure is formed by positioning the carrier wafer to be in contact with the oxide layer (col. 1, lines 45-50). Finally, pertaining to claim 10, Neudeck teaches the method, wherein a sacrificial oxide layer is formed on the Si-containing layer. (col. 5, lines 35-36)

However, Neudeck fails to show, pertaining to claims 6-8, performing a bonding step, the bonding step comprising heating at a temperature of from about 900°C to about 1100°C for a time period of about 1.5 hours to about 2.5 hours or performing the bonding step at a temperature from about 188° to about 27°C in the presence of an inert ambient; Neudeck also fails to show, pertaining to claim 9, the method wherein the channel region is formed by ion implantation and annealing; Neudeck fails to show, pertaining to claim 10, the method wherein, a sacrificial oxide layer is formed on the Si-containing layer prior to the ion implantation; Neudeck fails to show, pertaining to claim 11, the sacrificial spacers having a width of about 50 to about 100 nm; Finally, Neudeck fails to show, pertaining to claim 12, the undercutting shallow trench isolation regions formed by the steps of: chemical etching, isotropic reactive ion etching, oxidation and a second isotropic etch.

Komatsu teaches in figures, 1-12, and corresponding text, in a similar semiconductor method including a front and back gate device having a SOI substrate, the fabrication of SOI substrate that includes a bonding and annealing process. In addition, Komatsu teaches the use of

a resist pattern formed on a silicon wafer illustrating undercutting trenches that include the following: reactive ion etching, thermal oxidation process, and two wet etching techniques (col. 2, lines 60-61; col. 3, lines 1-5; col. 7, lines 26-35). Komastu also teaches a channel region formed by ion implantation and annealing.

It would have been obvious to one of ordinary skill in the art to incorporate the claimed bonding step, temperatures, and time periods, pertaining to claims 6-8, in the method of Neudeck, according to the teachings of Komatsu, with the motivation that, as stated in Komatsu, col. 1, lines 47-67; col. 2, lines 1-12, bonding methods are well known conventional processes used to fabricate Silicon-On-Insulator (SOI) substrates.

It would have been obvious to one of ordinary skill in the art to incorporate the ion implantation and annealing technique to the channel regions; and to form a sacrificial oxide layer on the Si-containing layer prior to the ion implantation, pertaining to claims 9 and 10, in the method of Neudeck, according to the teachings of Komatsu, with the motivation that, as stated in Komatsu, col. 2, lines 57-61; col. 7, lines 12-18, this technique is specifically drawn to forming an silicon active layer for a transistor device, where the material of this layer is made of a doped single crystal silicon, having either N-type or P-type impurities. In addition, Neudeck does teach that forming a sacrificial oxide layer on the Si-containing layer, prior to the ion implantation step, would be obvious for the purpose of protecting the Si-containing from contamination due to ion implantation techniques.

It would have been obvious to one of ordinary skill in the art to incorporate the width of the sacrificial spacers, pertaining to claim 11, in the method of Neudeck, as stated in Neudeck, col. 5, lines 54-59, since Neudeck includes the use of well known conventional techniques, such

as reactive-ion-etch (RIE) to form the nitride spacers, for the purpose of protecting the gate dielectric, the front-gate, and oxide from contamination due to a subsequent etching process. Thus, the claimed thickness would be appropriate to protect these layers from contamination.

Allowable Subject Matter

Claim 12 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to teach or render obvious the method "wherein said undercutting shallow trench isolation regions are formed by the steps of: chemical etching, isotropic reactive ion etching, oxidation, and a second isotropic etch."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
August 2, 2004

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812